--In Fig. 2, this circuit 5 comprises a timer circuit, which includes an n-channel MOS (nMOS) ~~nMOS~~ transistor M1 advantageously designed to have a very small drain-source leakage current, i.e. of minimum drain perimeter and surface. This transistor has its drain connected to the ground through another nMOS transistor 27, the gate of which is coupled to a discharge control input Dchrg. The drain of transistor M1 is also coupled through a diode D1 reverse-connected to the drain of a p-channel MOS (pMOS) ~~pMOS~~ transistor 24 having its source coupled to the voltage source V_{dd}. The gate of transistor 24 is connected to the output of an inverter 25 whose input is connected to the output of an OR gate 23. This OR gate 23 has a first input connected to the charge control input Chrg of circuit 5, and a second input connected to output Q of circuit 5.--

Please replace the paragraph beginning at page 8, Line 26 with the following rewritten paragraph:

--Additionally, the source of transistor M1 is connected, on the one hand, to the ground through a capacitor C, and on the other hand, to output Q of circuit 5 through two series-connected inverter stages for transforming the voltage across capacitor C into a logic signal. Conventionally, each inverter stage comprises a pMOS transistor 28 ~~20~~, 30, and an nMOS transistor 29, 31, which are series-connected between voltage source V_{dd} and the ground. Transistors 21 to 31 are constructed so that a very small voltage across the capacitor provides a logic level 1 at output Q.--

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